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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/636,466	08/11/2000	Woon-Yong Park		8876

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/636,466	Applicant(s) PARK, WOON-YONG	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 8/11/2000 is acceptable.

Drawings

The formal drawings filed on 8/11/2000 are acceptable.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Objections

Claims 1-10 are objected to because of the following informalities: Claim 1 recites the limitation "the upper peripheral region" and "the lower peripheral region" in lines 9 and 13. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of a peripheral area having an upper region above the display area and a lower region below the display area, as recited in claim 1, is unclear as to how the peripheral area having an upper region located above the display area and a lower region located below the display area when the peripheral area surrounds the display area and the drawings depict the upper and lower repair lines being formed in one plane.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,380,992).

Lee teaches in figure 7 and related text a thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate 99, 101 (figure 4b) with a display area and a peripheral area surrounding the display area, the peripheral area having an upper region above the display area and a lower region below the display area (figure 8);

signal lines 120, 121 (layers 121 are considered as part of the signal lines) formed on the substrate such that the signal lines are bundled into a plurality of blocks, each block having a predetermined number of signal lines;

a plurality of first upper repair lines 220a 220b (the upper part of lines 220a, 220b) formed at the upper peripheral region of the substrate, crossing one or more blocks of the signal lines;

a plurality of second upper repair lines 220a 220b (the lower part of lines 220a, 220b) formed at the upper peripheral region of the substrate, crossing all of the signal lines (in that block);

a plurality of upper connection members (the vertical connections connecting the upper part of lines 220a, 220b to the lower part of lines 220a, 220b) crossing the first upper repair lines and the second upper repair lines.

Lee does not teach in the embodiment of figure 7 a plurality of first lower repair lines formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines, the first lower repair lines crossing the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower peripheral region of the substrate, crossing all of the signal lines; and

a plurality of lower connection members (the block of group 131) crossing the first lower repair lines and the second lower repair lines.

Lee teaches in figure 1 the entire device wherein the lower peripheral region of the substrate is identical to the upper peripheral region of the substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use repair lines in the lower peripheral region of the substrate being identical to the upper peripheral region of the substrate, such that a plurality of first lower repair lines formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines, the first lower repair lines crossing the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower peripheral region of the substrate, crossing all of the signal lines; and

a plurality of lower connection members (the block of group 131) crossing the first lower repair lines and the second lower repair lines in Lee's device, in order to provide better capabilities to the device. Note that since the upper and lower repair lines are connected to the signal lines, then the first lower repair lines are indirectly connected to the corresponding first upper repair lines, as claimed.

Regarding claims 2, 4 and 9, the device of Lee includes a plurality of first and second interconnection lines (signal lines) interconnecting the first upper repair lines and the first lower repair lines, wherein the first and second interconnection lines are formed on a printed circuit board.

Regarding claim 3, Lee does not teach connecting the first upper repair lines to pins. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the first upper repair lines to two or more dummy pins of integrated circuits in Lee's device in order to provide conventional external connections to the device. Note that the repair lines are linked to the first interconnection lines.

Regarding claim 5, Lee teaches in figure 7 a plurality of third upper repair lines 210a, 21b formed at the upper peripheral region of the substrate while crossing the upper connection members and all of the signal lines; and
a plurality of third lower repair lines (the lower block of repair lines 210a, 210b formed at the lower peripheral region of the substrate while crossing the lower connection members and all of the signal lines.

Regarding claim 6, Lee teaches in figure 7 that each block of the signal lines comprises the signal lines connected to one of the integrated circuits.

Regarding claims 7 and 8, the device of Lee includes first upper and lower repair lines cross two blocks of the signal lines, wherein one or more of the upper and lower connection members are formed at each block of the signal lines.

Regarding claim 10, Lee does not teach using the device with a signal amplifying circuit. It would have been obvious to a person of ordinary skill in the art at the time the

invention was made to use the device with a signal amplifying circuit in the first and second interconnection lines in order to use the device in an application which requires a signal amplifying circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-I are cited as being related to TFT comprising repair lines.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
12/15/03

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800